Claims

Please amend claims as follows:

Claims 1-20 (canceled)

21. (currently amended) A method for reducing the ~~size~~ thickness of ~~at least a~~ an entire semiconductor ~~unit~~ chip or die in a process of making a package including a carrier and said semiconductor ~~unit~~ chip or die, said semiconductor ~~unit~~ chip or die including a first surface and a second surface, said second surface having no electrical connection device thereon, said carrier being physically separate from said semiconductor chip or die, said method comprising:

attaching permanently at least a part of said first surface to said carrier according to a configuration of lead-on-chip packaging; and

etching said semiconductor ~~unit~~ chip or die from said second surface to reduce the thickness of said semiconductor ~~unit~~ chip or die until the thickness of said semiconductor ~~unit~~ chip or die meets an expected specification.

22. (currently amended) The method according to claim 21 wherein said semiconductor ~~unit~~ chip or die is etched by using beams of light.

23. (currently amended) The method according to claim 21 wherein said semiconductor ~~unit~~ chip or die is etched by using plasma.

24. (currently amended) The method according to claim 21 wherein said expected specification means that the thickness of said semiconductor ~~unit~~ chip or die measured relative to said first surface is within a specified range.

25. (currently amended) The method according to claim 21 wherein said semiconductor ~~unit~~ chip or die is a wire bonding chip.

26. (currently amended) The method according to claim 21 wherein etching comprises a step of shielding at least a part of said semiconductor ~~unit~~ chip or die and said carrier to prevent the quality of said semiconductor ~~unit~~ chip or die and said carrier from being affected.

27. (currently amended) The method according to claim 21 further comprising, before attaching, grinding said semiconductor ~~unit~~ chip or die until the size thereof approximates said expected specification.

28. (currently amended) The method according to claim 21 wherein etching comprises ~~a step of~~ using a fixture to shield at least a part of said semiconductor ~~unit~~ chip or die and said carrier for preventing the quality of said semiconductor ~~unit~~ chip or die and said carrier from being affected.

29. (currently amended) The method according to claim 21 wherein said semiconductor ~~unit~~ chip or die is a wire bonding chip and is partly attached to said carrier via adhesive material.

30. (currently amended) The method according to claim 21 wherein said carrier is a chip carrier, said semiconductor ~~unit~~ chip or die includes at least an electrical connection device located on said first surface, and attaching includes connecting said electrical connection device to said chip carrier.

31. (currently amended) A method for reducing the ~~size~~ thickness of ~~at least a~~ an entire semiconductor ~~unit~~ chip or die in a process of lead-on-chip packaging wherein said semiconductor ~~unit~~ chip or die includes a first surface and a second surface, said first surface having at least an electrical connection device thereon, said second surface having no electrical connection device thereon, said method comprising:

attaching permanently said semiconductor ~~unit~~ chip or die to a ~~chip~~ carrier that is physically separate from said semiconductor chip or die, ~~in such a way that~~ with said

semiconductor ~~unit~~ chip or die and said ~~chip~~ carrier ~~are~~ in a configuration of lead-on-chip, ~~with~~ said first surface facing said carrier, and said second surface exposed; and

etching said semiconductor ~~unit~~ chip or die from said second surface to reduce the thickness of said semiconductor ~~unit~~ chip or die until the thickness of said semiconductor ~~unit~~ chip or die meets an expected specification.

32. (previously presented) The method according to claim 31 wherein etching includes applying beams of light on said second surface.

33. (currently amended) The method according to claim 31 further comprising, before attaching, grinding said semiconductor ~~unit~~ chip or die until the size of said semiconductor ~~unit~~ chip or die approximates said expected specification.

34. (currently amended) The method according to claim 31 wherein said expected specification means that the thickness of said semiconductor ~~unit~~ chip or die measured relative to said first surface is within a specified range.

35. (currently amended) The method according to claim 31 wherein said ~~configuration of lead-on-chip means that part of said~~ first surface is connectible with said chip carrier via adhesive material and said semiconductor ~~unit~~ chip or die is electrically connectible with said chip carrier via said electrical connection device.

36. (currently amended) The method according to claim 31 wherein attaching includes a step of connecting at least part of said first surface to said ~~chip~~ carrier via adhesive material.

37. (currently amended) The method according to claim 31 wherein etching comprises shielding at least part of said semiconductor ~~unit~~ chip or die and said carrier to prevent the quality of said semiconductor ~~unit~~ chip or die and said carrier from being affected.

38. (currently amended) The method according to claim 31 further comprising electrically connecting said semiconductor ~~unit~~ chip or die to said ~~chip~~ carrier via said electrical connection device after etching.

39. (currently amended) A method for reducing the ~~size~~ thickness of ~~at least a~~ an entire semiconductor chip or die ~~unit~~ in a process of packaging said semiconductor chip or die ~~unit~~ wherein said semiconductor chip or die ~~unit~~ includes a first surface and a second surface, said second surface having no electrical connection device thereon, said method comprising:

attaching permanently at least a part of said first surface to ~~said~~ a carrier that is physically separate from said semiconductor chip or die;

using a temporary, moveable fixture to surround said carrier and said semiconductor ~~unit~~ chip or die while ~~expose~~ exposing said second surface; and

etching said semiconductor chip or die ~~unit~~ from said second surface to reduce the thickness of said semiconductor chip or die ~~unit~~ until the thickness of said semiconductor chip or die ~~unit~~ meets an expected specification.

40. (currently amended) The method according to claim 39 wherein said carrier and said semiconductor chip or die ~~unit~~ are surrounded in such a way that said carrier and said semiconductor chip or die ~~unit~~ are shielded from etching except said second surface.